

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

(Use several sheets if necessary)

APPLICANT:
Svensson, et al.FILING DATE
12/5/97GROUP
2111

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER							ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
AB	AA	3	6	0	3	8	9	8	9/7/71	Dawson et al.			
AB	AB	5	0	9	5	2	2	3	3/10/92	Thomas			
AB	AC	5	3	3	9	2	3	6	8/16/94	Tamagawa			
	AD												
	AE												
	AF												
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	AH												
	AI												
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FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	AL							
	AM							
	AN							
	AO							
	AP							

OTHER DOCUMENTS (including Author, Title, Date, Place of Publication)

AB	AQ	Seitz, et al., "Hot-Clock nMOS", Proceedings of the 1985 Chapel Hill Conference on VLSI, pp. 1-17, 1985						
AB	AR	Koller, et al., "Adiabatic Switching, Low Energy Computing, and the Physics of Storing and Erasing Information", Proceedings of the Workshop on Physics and Computation (Physcomp '92), IEEE Press, pp. 1-5, 1993						
AB	AS	Younis, et al., "Practical Implementation of Charge Recovering Asymptotically Zero Power CMOS", Proceedings on the 1993 Symposium on Integrated Systems, MIT Press, pp. 234-250, 1993						

EXAMINER

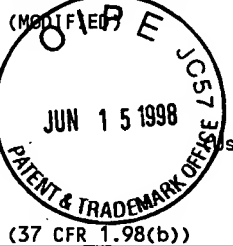
A. BERTHANE

DATE CONSIDERED

8/99

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SUBSTITUTE FORM-PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
06666/013001SERIAL NO.
08/986,327INFORMATION DISCLOSURE
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OTHER DOCUMENTS (including Author, Title, Date, Place of Publication)

AB	AQ	Athas, et al., "An Energy-Efficient CMOS Line Driver Using Adiabatic Switching", <u>IEEE Great Lakes Symposium on VLSI</u> , 1994
AB	AR	Mead et al., "Introduction to VLSI Systems, Chapter 1, MOS Devices and Circuits", <u>Addison-Wesley</u> , pp. 1-37, 1980
AB	AS	Weste et al., "Principles of CMOS VLSI Design, a Systems Perspective, Chapter 5, CMOS Circuit and Logic Design", <u>Addison-Wesley</u> , Second Edition, pp. 160-231, 1993

EXAMINER	A. BERTHANE	DATE CONSIDERED	8797
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AB	AQ	Nordin, et al., "A systems Perspective on Digital Interconnection Technology", <u>IEEE Journal of Lightwave Technology</u> , Vol 10, No. 6, pp. 811-827, June 1992
AB	AR	Slater, "MIPS Preview 64-Bit R4000 Architecture", <u>Microprocessor Report</u> , Vol. 5, No. 2, February 6, 1991
AB	AS	Svensson et al., "Adiabatic Charging Without Inductors", <u>USC/ISI Technical Report AC MOS-TR-3</u> , December 17, 1993

EXAMINER A. BERHANE

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AB	AQ	Athas et al., "An Energy-Efficient CMOS Line Driver Using Adiabatic Switching", <u>USC/ISI Technical Report ACMOS-TR-2a</u> , November 3, 1993
AB	AR	Chandrakasan, et al., "Low-Power CMOS Digital Design", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 27, No. 4, pp. 473-484, April 1992
AB	AS	Burr, et al., "Energy Considerations in Multichip-Module based Multiprocessors", <u>IEEE International Conference on Computer Design</u> , pp. 593-600, 1991

EXAMINER A. BERTHANEDATE CONSIDERED 8/99

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INFORMATION DISCLOSURE CITATION
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Atty. Docket No. 07067.0008				Serial No. 08/986,327			
Applicant Lars SVENSSON et al.							
Filing Date December 5, 1997				Group 2838			
U.S. PATENT DOCUMENTS							
Examiner Initial*		Document Number	Date	Name	Class	Sub Class	Filing Date If Appropriate
B	<input checked="" type="checkbox"/>	5,459,414	10/17/95	Dickinson	11	11	
	<input checked="" type="checkbox"/>	5,473,269	12/05/95	Dickinson	11	11	
	<input checked="" type="checkbox"/>	5,506,520	04/09/96	Frank et al.	11	11	
	<input checked="" type="checkbox"/>	5,517,145	05/14/96	Frank	11	11	
	<input checked="" type="checkbox"/>	5,521,538	05/28/96	Dickinson	11	11	
	<input checked="" type="checkbox"/>	5,526,319	06/11/96	Denhard et al.	11	11	
	<input checked="" type="checkbox"/>	5,602,497	02/11/97	Thomas	11	11	
	<input checked="" type="checkbox"/>	5,604,454	02/18/97	Maguire et al.	11	11	
	<input checked="" type="checkbox"/>	5,675,263	10/07/97	Gabara	11	11	
<input checked="" type="checkbox"/>	5,838,203	11/17/98	Stamoulis et al.	11	11		
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Sub Class	Translation Yes or No
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
Mateo, D., et al. "Quasi-adiabatic ternary CMOS logic", Electronics Letters, Vol. 32, No. 2, 1/18/96. COPY NOT PROVIDED (CNP)							
Younis, Saed, et al., "Non-Dissipative Rail Drivers for Adiabatic Circuits", IEEE, p.404-414, 1995 (CNP)							
Dickinson, Alex, et al., "Adiabatic Dynamic Logic", IEEE, p.282-285, 1994 CNP							
Ye, Yibin, et al. "Energy Recovery Circuits Using Reversible and Partially Reversible Logic", IEEE p.769-778, 1996. COPY NOT PROVIDED							
Examiner A-BERHANE				Date Considered 8/99			
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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U.S. PATENT DOCUMENTS							
Examiner Initial*	Document Number	Date	Name	Class	Sub Class	Filing Date If Appropriate	
AB	5,841,299	11/24/98	De				
AB	5,870,331	02/09/99	Hwang et al.				
AB	5,880,602	03/09/99	Kaminaga et al.				
AB	5,889,439	03/30/99	Meyer et al.				
AB	5,881,014	03/09/99	Ooishi				
AB	5,883,538	03/16/99	Keeth et al.				
FOREIGN PATENT DOCUMENTS							
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